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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/772,830	01/30/2001	Frank K. Baker JR.	SC11150TH	2027

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EXAMINER
NAMAZI, MEHDI

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/772,830	Baker, Jr. et al.
Examiner	**Art Unit**
Mehdi Namazi	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jan 30, 2001* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-14 and 16-20* is/are rejected.

7) ☒ Claim(s) *15* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *1-30-2001* is/are a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *4*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-20 are presented for examination. This office action is in response to the application filed on 01/30/2001.

Drawings

2. The drawings filed on January 30, 2001 are approved.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 6-10, 13, and 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Young et al.(Young)(U.S.Patent No. 5,285,421).

As per claims 1 and 16, Young teaches a memory system comprising: an array of addressable storage elements arranged in a plurality of rows and a plurality of columns(fig. 5, element 503); and decoding circuitry coupled to the array of addressable storage elements(fig. 6, X-decoder), the decoding circuitry, responsive to decoding a first address(fig. 6, X-decoder), to access a first storage element of a first row of the plurality of

rows, and the decoding circuitry, responsive to decoding a second address consecutive to the first address, to access a second storage element of a second row of the plurality of rows, the second row of the plurality of rows different from the first row of the plurality of rows (the memory has been divided into two blocks or halves independent of each other, so both blocks are accessed simultaneously but two different rows of memory)(col. 4, lines 52-68).

As per claims 2, 8, Young teaches each of the storage elements stores one bit(col. 4, lines 48-50, memory 50 in fig. 5, is made of plurality of word lines, where each word line is made of plurality of bits and each bit is stored in one memory cell).

As per claims 3, 9, Young teaches each of the storage elements stores a plurality of bits arranged as a word (col. 4, lines 58-61, where during the initial access of the memory 50, it loads eight bytes of data into the register. That means storing two words, where each word is made of four bytes).

As per claims 4, 10 , Young teaches each of the storage elements stores a plurality of bits arranged as a page (col. 4, lines 58-61, where during the initial access of the memory 50, it loads eight bytes of data into the register. That means storing

two words or one page, where each page is made of plurality of words and each word contains plurality of bits).

As per claim 17, Young teaches accessing a first storage element comprises reading a first page, the first page comprising a plurality of bits(col. 4, lines 67-62, where both halves of the memory with the same row address with a total of eight bytes or one page is going to be accessed simultaneously).

As per claim 6, Young teaches a memory system comprising: an array of storage elements arranged in a plurality of rows and a plurality of columns(fig. 6, shows plurality of rows and it is inherent to have plurality of columns), each of the storage elements comprising an input and an output(inherent), each of the storage elements corresponding to a numeric address comprising more significant bits and less significant bits(rows and columns represent most significant and less significant bits); a column decoder coupled to the outputs of the storage elements of each of the plurality of columns(fig. 6, shows the row decoder but does not show the column decoder, but it is inherent to have a column decoder), the column decoder operable responsive to at least one of the more significant bits(columns represent most significant bits, A0-A2); and a row decoder coupled to the inputs of the storage elements of each of the plurality of rows(fig. 6), the

row decoder operable responsive to at least one of the less significant bits(col. 4, lines 42-43).

As per claim 7, Young teaches wherein the input of each of the storage elements is a control gate, and the output of each of the storage elements is a drain(inherent).

As per claim 13, Young teaches wherein the at least one of the less significant bits comprises all of the less significant bits(col. 4, lines 42-43).

As per claim 18, Young teaches wherein accessing a second storage element comprises reading a second page different from the first page, the second page comprising a plurality of bits(accessing second row represent second page with plurality of bits).

As per claim 19, Young teaches wherein accessing a first storage element comprises initiating a first burst access, the first burst access comprising a plurality of bits(col. 4, lines 65-68).

As per claim 20, Young teaches wherein accessing a second storage element comprises initiating a second burst access different from the first burst access, the second burst access comprising a plurality of bits(col. 4, lines 65-68).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 11-12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Young, and further in view of Lee et al.(Lee)(U.S.Patent No. 5,920,504).

As per claim 14, Young teaches an embedded control system comprising: a processor(fig. 5, element 401); and a memory system coupled to the processor(fig. 5, element 503), the memory system comprising an input to receive an address signal from the processor(fig. 5, element 14), an output to send addressed information to the processor(fig. 5, element 32), and a plurality of blocks(fig. 6), each of the plurality of blocks comprising: an array of memory cells arranged in a plurality of rows and a plurality of columns (the basic structure of any memory is made of rows and columns)to store information within a plurality of pages(any row or column is made of plurality of cells where each row is made of a page) , each of the plurality of pages

comprising a plurality of words(inherent), each of the plurality of words comprising a plurality of bits(inherent); and decoding circuitry comprising a column decoder and a row decoder(fig. 3, elements 301 and 302) , the decoding circuitry coupled to the input(fig. 3), the output and the array of memory cells(fig. 3), the decoding circuitry, responsive to the address signal having a first address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second address consecutive to the first address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output (the memory has been divided into to blocks or halves independent of each other, so both blocks are accessed simultaneously but two different rows of memory)(col. 4, lines 52-68).

As per claims 5, 11, Young teaches the claimed invention as detailed above in the previous paragraph, but fails to teach a storage with plurality of nonvolatile memory cells.

Lee similarly discloses a storage with plurality of memory cells, wherein each memory cell is able to conserve data even when there is no power supply(col. 1, lines 9-10). In this way

Lee teaches a storage with plurality of nonvolatile memory cells, in order to preserved data from erasure.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to use a nonvolatile memory, wherein nonvolatile memory is able to conserve data even when there is no power supply, as taught by Lee into system of Young in order to preserve data from erasure in case of power shortage. One ordinary skill in the art would found ample suggestion therein to modify the Young system by providing a plurality of nonvolatile memory cells, where each memory cell can preserve one bit of data in event of power failure.

As per claim 12, Lee teaches wherein each of nonvolatile memory cells comprises a floating-gate type cell(col. 5, lines 61-63).

Allowable Subject Matter

7. Claim 15 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,715,421 (*Akiyama et al.*)teaches an apparatus and method of addressing paged mode memory including adjacent page precharging.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is (703) 306-2758. The examiner can normally be reached on Monday-Friday from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Hyun Yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Any response to this action should be mailed to:

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or faxed to:

(703) 308-9051-2, (for formal communications intended for entry)

Or:

(703) 305-6606 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park 2, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

Reginald G. Bragdon

REGINALD G. BRAGDON
PRIMARY EXAMINER

M. Namazi
Patent Examiner
Art Unit 2188
November 14, 2002